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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,695	12/17/2001	Hiroshi Kume	31762-177289	6299

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,695	KUME ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 6/14/05. Claims 1-23 have been cancelled. Claims 24-25 are currently pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. *Claim 25 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.*

The instant claim recites "letting data stored in said shift register be written into said reception FIFO circuit, when the second interrupt signal is input thereto"; however, there is no support for this feature in the specification or in the drawings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (US 6378011 B1) in view of well-known features, as evidenced by Firoozmand (US 5210749 A).*

Regarding claim 24, Moore discloses a FIFO controller (e.g., Fig. 1, "ASD Rx Control 108" and "ASD Tx Control 107") connected to a second bus (e.g., col. 6, lines 25-27, "DSP Interface Bus"); a transmission controller with the first write pointer controller outputting the first write count signal (e.g., col. 6, lines 25-29, "[f]ollowing a single parallel write ... the ASD Register Module 101 increments the ASD Tx FIFO Fill Level Register (ATFFL) 151"); a reception controller with the second write pointer controller outputting the second write count signal (e.g., col. 7, lines 18-22, "the byte is received... [t]he ASD Rx FIFO Fill Level register (ARFFL) 161) is then incremented"), a trigger detector comprising a transmission trigger detector (e.g., Fig. 1, "ATFFL"; col. 6, line 28, "ASD Tx FIFO Fill Level Register") and reception trigger detector (e.g., Fig. 1, "ARFFL"; col. 7, lines 21-22, "ASD Rx FIFO Fill Level Register"), the transmission trigger detector outputting a first interrupt output control signal when a count value is equal to a first predetermined value indicating a remaining data amount (e.g., col. 4, lines 35-38, "thresholds for interrupts are contained in... ASD Tx FIFO Threshold Register"); the reception trigger detector outputting a first interrupt output control signal when a count value is equal to a first predetermined value indicating a remaining data amount (e.g., col. 4, lines 35-38, "thresholds for interrupts are contained in... ASD Rx

FIFO Threshold Register"); a transmission FIFO circuit connected to the second data bus to store first data input from the bus buffer circuit (e.g., col. 6, lines 30-32); and a reception FIFO circuit for reading out the stored second data (e.g., col. 7, lines 20-21, "128x8 FIFO buffer", "retrieve the data in a parallel fashion") and storing data from the shift register connected to an external bus (e.g., col. 7, lines 15-18, "ASDI" pin is serial bus whose input is shifted to form data); an internal interrupt circuit connected to the second data bus for outputting a first interrupt signal when the first interrupt output control signal is input (e.g., Fig. 1, "Interrupt Gen 114"); and an interrupt circuit connected to the first data bus for generating a first internal interrupt signal (e.g., col. 4, lines 12-15, "DSP interface including the IRQ signals"), and a central processor letting data stored in the bus buffer circuit be written into the FIFO when the first interrupt signal is input thereto (e.g., col. 10, lines 32-36; col. 7, lines 36-38; col. 4, lines 36-38, "thresholds for interrupts"). Moore does not expressly mention outputting first and second read count signals; however this is implicit in the description of the Fill Level Registers cited above. Specifically, Moore teaches that the Fill Level Registers allow "determine[ing] the number of reads or writes necessary to empty or fill the FIFO" (col. 7, lines 45-47). Thus by expressly disclosing incrementing their values when data is added, and with the understanding that data is also removed from the FIFOs to which they pertain, it is implicit that these values are also decremented. Thus the signals that decrement the Fill Level Registers are implicit and their operation is derived from an understanding of the Fill Level Register function as disclosed by Moore.

Moore also discloses that byte data is stored to a 128x8 Tx FIFO (e.g., col. 6, lines 30-32) and storing to a 128x8 Rx FIFO (e.g., col. 7, lines 19-21). Moore does not expressly mention that an address pointer designates the address where the data is stored; however the Examiner takes Official Notice that a pointer is widely used to designate a particular location, as among the 128 positions of Moore, in which to place data when the structure is important as in the FIFO of Moore. This finds evidence in Firoozmand who teaches the use of pointers to address a storage location in a FIFO in order to write data (e.g., col. 5, lines 11-15).

3. *Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore as applied in the parent claim, further in view of Lewis (US 5619544 A).*

Regarding claim 25, Moore also discloses the interrupt circuit generating a second interrupt signal (e.g., col. 4, lines 12-15, "DSP interface including the IRQ signals" which are output according to the threshold interrupt of the ASD Rx FIFO Threshold Register, see col. 4, lines 35-37). Moore also discloses letting data stored be written when an interrupt signal is input (e.g., col. 3, lines 56-58; col. 4, lines 35-38, but for the transmission FIFO), but does not expressly mention a similar use for the reception FIFO; however, this feature is disclosed by Lewis, who discloses letting a data stored in a shift register (e.g., col. 5, lines 24-28, "asserted before resuming the transfer") be written into a reception FIFO (e.g., Fig. 2, "32 : SOUT" written to "Receive Data FIFO 47"). It would have been obvious to one of ordinary skill in the art to

combine Lewis with Moore, because Lewis provides a superior method of handling FIFO overruns by providing said indication (e.g., col. 5, lines 19-22).

Response to Arguments

Applicant's arguments filed 6/14/05 have been fully considered but they are not persuasive. Although new grounds of rejection introduced supra were necessitated by amendment, the arguments presented by the Applicant are relevant and thus are treated infra.

Regarding claim 24, Applicant argues that Moore does not disclose "an internal interrupt circuit connected to a second data bus, in combination with an interrupt circuit connected to a first data bus"; however, this feature, introduced by the Applicant in new claim 24, is seen in Moore as newly cited supra. In particular, as seen in Figure 1, the second bus connects Moore's FIFO controllers ("108") to the ASD Register Module ("101") which generates the internal interrupts that are passed on to the first bus, which comprises the DSP and its IRQ lines (e.g., col. 4, lines 12-15, "DSP interface including the IRQ signals"), while "the interrupt circuit connected" thereto is disclosed by the functioning of an IRQ in a processor. These features are hopefully clear from the detailed citation supra, which represents an interpretation of Moore that anticipates the all the features, including those newly introduced, in claim 24.

Thus new claims 24-25 are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk